

PTO/SB/08B (10-01)
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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) Sheet <input type="text"/> of <input type="text"/>		Complete if Known	
		Application Number	09/994,299
		Filing Date	NOVEMBER 26, 2001
		First Named Inventor	MIRON ABRAMOVICI
		Group Art Unit	2133
		Examiner Name	
		Attorney Docket Number	487-012

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
DT	1	C. STROUD, S. WIJESURIYA, C. HAMILTON, AND M. ABRAMOVICI, "Built-In Self-Test of FPGA Interconnect," Proc. Int'l. Test Conf., pp. 404-411, 1998.	
DT	2	I. HARRIS AND R. TESSIER, "Interconnect Testing in Cluster-Based FPGA Architectures", Proc. AMC/IEEE Design Automation Conf., 2000	
DT	3	I. HARRIS AND R. TESSIER, "Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures", Proc. IEEE Int'l Conf. on Computer Aided Design, 2000.	
DT	4	M. ABRAMOVICI, ET AL., "Using Roving STARS for On-Line Testing and Diagnosis of FPGAs in Fault-Tolerant Applications," Proc. IEEE Int'l. Test Conf., pp. 973-982, 1999.	
DT	5	M. ABRAMOVICI, ET AL., "Improving On-Line BIST-Based Diagnosis for Roving STARS," Proc. IEEE Int'l On-Line Testing Workshop, 2000.	
DT	6	K. ROY AND S. NAG, "On Routability for FPGAs Under Faulty Conditions," IEEE Trans on Computers, Vol. 44, pp. 1296-1305, 1995.	

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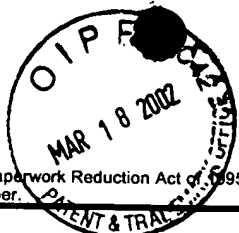
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DT	1	A. STEININGER AND SCHERRER, "On the Necessity of On-Line BIST in Safety Critical Applications," Proc. 29th Fault-Tolerant Computing Symp", pp. 208-215, 1999.	
DT	2	M. RENOVELL, J. PORTAL, J. FIGUERAS, AND Y. ZORIAN, "Testing the Interconnect of RAM-Based FPGA," Proc. IEEE Design & Test of Computers, Vol. 15, No. 1, pp. 45-50, 1998.	
DT	3	S. DUTT AND F. HANCHECK, "REMOD: A New Methodology for Designing Fault-Tolerant Arithmetic Circuits," IEEE Trans. on VLSI Systems, Vol. 5, pp. 34-56, 1997.	
DT	4	S. DUTT, ET AL., "Efficient Incremental Rerouting for Fault Reconfiguration in Field Programmable Gate Arrays," ACM/IEEE Int'l Conf. on Computer Aided Design, 1999.	
DT	5	J. EMMERT AND D. BHATIA, "Reconfiguring FPGA Mapped Designs with Applications to Fault Tolerance and Reconfigurable Computing", Lecture Notes on Comp. Sci., Vol. 1304, pp. 141-150, 1997.	
DT	6	J. EMMERT AND D. BHATIA, "A Fault Tolerant Technique for FPGAs", Journal of Electronic Testing, Vol. 16, pp. 591-606, 2000.	
DT	7	F. HANCHEK AND S. DUTT, "Methodologies for Tolerating Logic and Interconnect Faults in FPGAs," IEEE Trans.on Computers, pp. 15-33, 1998.	
DT	8	J. LACH, ET AL., "Low Overhead Fault-Tolerant FPGA Systems," IEEE Trans. on VLSI Systems, Vol. 6, No. 2, pp. 212-221, 1998.	
DT	9	J. LACH, ET AL., "Algorithms for Efficient Runtime Fault Recovery on Diverse FPGA Architectures," Proc. Int'l. Symp. on Defect and Fault Tolerance In VLSI Systems, 1999.	
DT	10	N. MAHAPATRA AND S. DUTT, "Efficient Network Flow Based Technique for Dynamic Fault Reconfiguration in FPGAs", Proc. Fault Tolerant Computing Symp., pp. 122-129, 1999.	

Examiner Signature	<i>Davidson</i>	Date Considered	3/11/02
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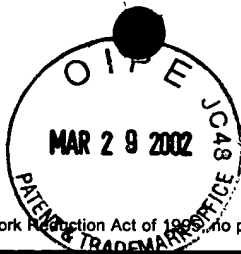
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Examiner Initials	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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